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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 3

Compl t if Kn wn	
Application Number	
Filing Date	
First Named Inventor	Cavanaugh
Group Art Unit	
Examiner Name	
Attorney Docket Number	62061.0105

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
AZ		5,202,889		Aharon, et al.	4/13/1993	
AZ		5,448,746		Eickemeyer, et al.	9/5/95	
AZ		5,983,335		Dwyer, III	11/9/99	
AZ		5,805,470		Averill	9/8/98	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature	Anne L. Damiano	Date Considered	9/16/03

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[1] Unique citation designation number. [2] See attached Kinds of U.S. Patent Documents. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

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Sheet 2 of 3

Complet if Known	
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Filing Date	
First Named Inventor	Cavanaugh
Group Art Unit	
Examiner Name	
Attorney Docket Number	62061.0105

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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
AZD		PARK, et al., Evaluation of Scheduling Techniques on a SPARC-Based VLIW Testbed, Proceedings of the 30th Annual International Symposium on Microarchitecture, Dec. 1997	
AZD		MORENO, et al., Simulation/evaluation environment for a VLIW processor architecture, IBM Journal of Research and Development, Vol. 41, No. 3 Received August 8, 1996; accepted for publication March 18, 1997	
AZD		LICHTENSTEIN, et al., Model Based Test Generation for Processor Design Verification", Sixth Innovative Applications of Artificial Intelligence Conference, August 1994.	
AZD		LICHTENSTEIN, et al., Test Program Generation for Functional Verification of PowerPC processors in IBM, IEEE/ACM 32'nd Design Automation Conference, June 1995	
AZD		AHARON, et al., Verification of the IBM RISC System/6000 by a dynamic biased pseudo-random test program generator, published in IBM Systems Journal, Vol. 30, No. 4, 1991	
AZD		CASAUBIEILH, et al., Functional verification methodology of Chameleon processor, presented at the 33rd Annual ACM IEEE Design Automation Conference, June 3 - 7, 1996	
AZD		BELLON, et al., Automatic Generation of Microprocessor Test Programs, presented at ACM IEEE Nineteenth Design Automation Conference Proceedings, June, 1982	
AZD		ANDERSON, Logical Verification of the NVAX CPU Chip Design, Digital Technical Journal of Digital Equipment Corporation, Vol. 4 No. 3, Summer 1992	
AZD		CHANDRA, et al., Constraint Solving for Test Case Generation - A Technique for High Level Design Verification, published in: International Conference on Computer Design: VLSI in Computers and Processors, Proceedings. Los Alamitos, IEEE Computer Society Press, 1992	
AZD		LOGAN, et al., Directions in Multiprocessor Verification, presented at the 14th Annual IEEE International Phoenix Conference on Computers and Communications, March, 1995	
AZD		RAGHAVAN, et al., Multiprocessor System Verification Through Behavioral Modeling and Simulation, presented at the 14th Annual IEEE International Phoenix Conference on Computers and Communications, March, 1995	

Examiner Signature	Anne L. Damiani	Date Considered	9/11/03

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Sheet 3 of 3

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First Named Inventor	Cavanaugh
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Examiner Name	
Attorney Docket Number	62061.0105

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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
AZA		SAHA, et al., A Simulation-Based Approach to Architectural Verification of Multiprocessor Systems, presented at the 14th Annual IEEE International Phoenix Conference on Computers and Communications, March, 1995	

Examiner Signature	Anne L. Damiano	Date Considered	9/16/03

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